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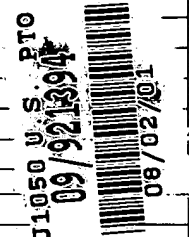
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				Application Number	TBD
				Filing Date	08/02/01
				First Named Inventor	Sudhir K. Madan
				Group Art Unit	TBD
				Examiner Name	TBD
				Attorney Docket No.	TI-30841
Sheet	1	of	1		



U.S. PATENT DOCUMENTS						
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OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
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DV	CA	"Highly Scalable and Fully Logic Compatible SRAM Cell Technology with Metal Damascene Process and W Local Interconnect," 0-7803-4700-6/98; 1998 IEEE; by M. Inohara, H. Oyamastu, Y Unno, Y FuKaura, S. Goto, Y. Egi, and M. Kinugawa.	
DV	CB	"A Novel 6.4μm ² Full-CMOS SRAM Cell with Aspect Ratio of 0.63 in a High-Performance 0.25 μm-Generation CMOS Technology"; 0-7803-4700-6/98; 1998 IEEE; by K. J. Kim, J. M. Younn, S. B. Kim, J. H. Kim, S. H. Hwang, K. T. Kim, and Y. S. Shin.	
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12/21/04